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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/512,016	06/27/2005	Hans-Joachim Barth	10808/163	8447
48581	7590	08/28/2009	EXAMINER	
BRINKS HOFER GILSON & LIONE/INFINEON INFINEON PO BOX 10395 CHICAGO, IL 60610			VELASQUEZ, VANESSA T	
ART UNIT	PAPER NUMBER		1793	
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b> 10/512,016	<b>Applicant(s)</b> BARTH ET AL.
	<b>Examiner</b> Vanessa Velasquez	<b>Art Unit</b> 1793

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If no period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED. (35 U.S.C. § 133).

Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

1) Responsive to communication(s) filed on 23 June 2009.  
 2a) This action is FINAL.      2b) This action is non-final.  
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

4) Claim(s) 12-26 is/are pending in the application.  
 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
 5) Claim(s) \_\_\_\_\_ is/are allowed.  
 6) Claim(s) 12-26 is/are rejected.  
 7) Claim(s) \_\_\_\_\_ is/are objected to.  
 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

9) The specification is objected to by the Examiner.  
 10) The drawing(s) filed on 27 June 2005 is/are: a) accepted or b) objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) All    b) Some \* c) None of:  
 1. Certified copies of the priority documents have been received.  
 2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

1) Notice of References Cited (PTO-892)  
 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)  
 3) Information Disclosure Statement(s) (PTO/06/08)  
 Paper No(s)/Mail Date \_\_\_\_\_

4) Interview Summary (PTO-413)  
 Paper No(s)/Mail Date \_\_\_\_\_  
 5) Notice of Informal Patent Application  
 6) Other: \_\_\_\_\_

**DETAILED ACTION**

***Continued Examination Under 37 CFR 1.114***

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on June 23, 2009 has been entered.

***Status of Claims***

Claims 1-11 are canceled. Claims 23-26 are newly added. Currently, claims 12-22 are pending and presented for examination.

***Status of Previous Objections***

The previous objection to claim 18 for not specifying a unit of measure is withdrawn in view of the amendment to the claim.

***Claim Objections***

Claim 14 is objected to because of a possible typographical error. It is believed that "second direction" (last line of the claim) is supposed to be "secondary direction."

Claim 23 is objected to because of what appears to be a grammatical error in the phrase "features size" as read in the context of the claim. Claim 23 is further objected to because "um" is not a proper abbreviation for micrometer ( $\mu\text{m}$ ).

***Claim Rejections - 35 USC § 112, First Paragraph***

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 18, 25, and 26 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claims contain subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention.

Regarding claim 18, the claim recites that the impurity proportion is less than 5% by weight. There is no support in the original disclosure that the unit of measure is weight percent.

Regarding claim 25, the claim recites that the movement of the thermal region is conducted at a rate of "approximately 1 cm/second." There is no support in the specification for the term "approximately" with regard to a rate of 1 cm/second. It should

be noted that use of the term "approximately" broadens the scope of the claim because "approximately" encompasses rates close to or about 1 cm/second (e.g., 0.8, 0.97, and 1.15 cm/second), for which there is no original disclosure. Thus, the claim does not comply with the written description requirement.

Regarding claim 26, the claim is likewise rejected for being dependent on rejected independent claim 25.

***Claim Rejections - 35 USC § 102***

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 12, 13, 14, 18, 19, 21, 23, 24 are rejected under 35 U.S.C. 102(b) as being anticipated by Gat et al. (US 4,214,918).

Regarding claims 12, 23, and 24, Gat et al. teach a process for forming connection patterns (interconnection) of low resistance semiconductor materials (abstract). The process includes the following steps: (1) depositing semiconductor material (e.g., polysilicon layer **6**) on a substrate (carrier material) comprising silicon **2** and silicon nitride **4** (col. 2, lines 60-65; Fig. 1), the semiconductor material having an initial (first) grain size of 300-600 Å ("SAMPLES" Table; col. 3, lines 23-24); and (2) scanning (moving) a laser beam (source of thermal energy) across the semiconductor material and substrate in the X and Y directions (col. 3, lines 9-14). After laser

scanning, the grains of the polysilicon grow from 300-600 Å (first grain size) to 25 µm (second grain size) ("SAMPLES" Table; col. 3, lines 22-30). The coarsened grains are lengthened with respect to the initial grains, as inherently demonstrated by the increase of grain size from angstrom-scale to micron-scale, with even some grains growing to be as long as 32 µm (col. 3, lines 25-29). It is noted that the semiconductor material that forms the interconnect may be characterized as being "finely-patterned" because of its nano-scale thickness of 500 nm (col. 2, lines 63-65) and angstrom-scale grain sizes of 300-600 Å ("SAMPLES" Table; col. 3, lines 23-24). It is further noted that the semiconductor material may include metals such as molybdenum, platinum, and tungsten (col. 5, lines 26-32).

Regarding claims 13 and 23, the interconnection has an average grain size of 550 Å (0.055 µm) (col. 3, lines 21-23). This teaching anticipates the claim because it is a specific value that lies within the claimed range (MPEP § 2131.03(l)).

Regarding claim 14, the deposited polycrystalline silicon (interconnection) on substrate is cut into a square measuring 5 mm by 5 mm (col. 3, lines 2-6). It is noted that the act of cutting inherently requires the forming (cutting) process to occur in at least one direction. With regard to the movement of the laser beam, Gat et al. teach that the laser beam is scanned in X and Y directions, which is conventionally understood to be parallel to the edges of the square and planar substrate, and also signifies that scanning is conducted along the edges of the cut (i.e., the direction in which the polycrystalline silicon is formed by cutting).

Regarding claim 18, Gat et al. do not teach the presence of impurities (i.e., unwanted or undesirable components). Thus, they will be presumed to be absent (i.e., zero percent) or present only in negligible amounts. Note that the claimed range includes zero percent (5% or less). Therefore, Gat et al. anticipate the claim limitation.

Regarding claim 19, the silicon nitride **4** and silicon oxide **12** layers function as diffusion barrier layers because their non-conductive properties prevent interaction between semi-conductive layers **2 & 4** and **10 & 14**, respectively (Fig. 1; Fig. 2b).

Regarding claim 21, the substrate and semiconductor layer thereon have temperatures of 250-350°C as the laser is scanned across their surface (col. 3, lines 17-20). The range disclosed by the prior art lies clearly and completely within the claimed range; thus, the prior art anticipates the claimed range because the prior art discloses the claimed range with "sufficient specificity" (MPEP § 2131.03(II)).

#### ***Claim Rejections - 35 USC § 103***

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148

USPQ 459 (1966), that are applied for establishing a background for determining

obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

8. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

9. Claims 16, 17, 22, 25, and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gat et al. (US 4,214,918), as applied to claim 12 above, and further in view of Fan et al. (US 4,509,461).

Regarding claims 16 and 17, Gat et al. teach that the source of energy to promote recrystallization may be a laser beam (col. 2, lines 20-24), but they are silent as to the shape of the beam. However, the shape of the beam is arbitrary, and in particular, the claimed shape of a "strip-type" and "fanned-out" laser is already well-

known in the recrystallization arts. U.S. Patent 4,059,461, issued to Fan et al. and drawn to enhancing the crystallinity of semiconductor films, teaches that the preferred shape of the laser endpoint is laser is an elongated slit (strip-type, fanned-out in the sense that the beam endpoint is spread out) (col. 4, lines 14-35). While other shapes may be utilized, the elongated slit is particularly preferred because it enables the crystals to form in a certain, desired spatial arrangement (Fan et al., col. 4, lines 22-27). Thus, it would have been obvious to one of ordinary skill in the art to form the laser beam endpoint in Gat et al. into the shape of an elongated slit for the purpose of inducing stresses that enable the recrystallized semiconductor to possess a desired orientation, as taught by Fan et al.

Regarding claim 22, Gat et al. are silent as to the type of atmosphere under which the recrystallization process occurs. However, it is well known in the art that laser scanning may be conducted in an environment such that oxidation of the substrate and sample does not occur (i.e., a protective atmosphere), as evidenced by Fan et al. (col. 3, lines 36-40). Thus, it would have been obvious to one of ordinary skill in the art to have implemented the controlled atmosphere of Fan et al. in the process of Gat et al. for the purpose of preventing oxidation of the substrate being treated.

Regarding independent claim 25 and claim 26, Gat et al. teach a process for forming connection patterns (interconnection) of low resistance semiconductor materials (abstract). The process includes the following steps: (1) depositing semiconductor material (e.g., polysilicon layer **6**) on a substrate (carrier material) comprising silicon **2** and silicon nitride **4** (col. 2, lines 60-65; Fig. 1), the semiconductor material having an

initial (first) grain size of 300-600 Å ("SAMPLES" Table; col. 3, lines 23-24); and (2) scanning (moving) a laser beam (source of thermal energy) across the semiconductor material and substrate in the X and Y directions (col. 3, lines 9-14). After laser scanning, the grains of the polysilicon grow from 300-600 Å (first grain size) to 25 µm (second grain size) ("SAMPLES" Table; col. 3, lines 22-30). The coarsened grains are lengthened with respect to the initial grains, as inherently demonstrated by the increase of grain size from angstrom-scale to micron-scale, with even some grains growing to be as long as 32 µm (col. 3, lines 25-29). It is noted that the semiconductor material that forms the interconnect may be characterized as being "finely-patterned" because of its nano-scale thickness of 500 nm (col. 2, lines 63-65) and angstrom-scale grain sizes of 300-600 Å ("SAMPLES" Table; col. 3, lines 23-24). It is further noted that the semiconductor material may include metals such as molybdenum, platinum, and tungsten (col. 5, lines 26-32).

Further regarding claims 25 and 26, Gat et al. do not teach the claimed scanning rate. However, those of ordinary skill in the art would recognize that discovering an optimum scan rate requires nothing more than routine optimization, as evidenced by Fan et al. (col. 5, lines 3-5). Fan et al. teach that the scan rate is determined by the "dwell time" (duration of the laser on the surface of the sample), which is further influenced by parameters including, but not limited to, the power of the laser, the efficiency of the laser, and the spot size of the laser (col. 4, lines 65-68 to col. 5, lines 1-2). Additionally, it is taught that the dwell time, and thus the scan rate, affects the extent to which the sample is crystallized (col. 5, lines 10-13). Therefore, it would have been

obvious to one of ordinary skill in the art to have optimized the laser scan rate of Gat et al. in order to effect a desired degree of crystallinity. Furthermore, this optimization would not be considered inventive or even burdensome, as Fan et al. clearly teach that optimization requires no more than routine skill in the art (col. 5, lines 3-5; also MPEP § 2144.05).

10. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gat et al. (US 4,214,918), as applied to claim 12 above, and further in view of Wanlass (US 5,882,958).

Regarding claim 20, Gat et al. do not teach forming the polycrystalline silicon interconnections by a damascene method. However, the damascene procedure is a well-known patterning method for achieving a given transistor configuration, as evidenced by Wanlass. Wanlass teaches a method of damascene patterning a silicon-on-insulator MOS transistor, which is thereafter annealed to grow crystals in originally amorphous silicon (col. 1, lines 64-67 to col. 2, lines 1-9). It would have been obvious to one of ordinary skill in the art to have implemented the damascene patterning method of Wanlass into the method of Gat et al. because it is a conventional method for obtaining an arbitrary pattern of choice.

11. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gat et al. (US 4,214,918), as applied to claim 12 above, and further in view of Higuchi et al. (JP 61-30027, English abstract).

Regarding claim 15, Gat et al. do not explicitly teach repeating the movement of the thermal region. JP 61-30027, issued to Higuchi et al. and drawn to a process of recrystallizing semiconductors using an electron beam and heating lamp, teach repeating the recrystallization process for the purpose of recrystallizing the entire sample (English abstract). Therefore, it would have been obvious to one of ordinary skill in the art to have applied the act of repetition, as taught by Higuchi et al., to the laser scanning step of Gat et al. so that the entire surface area of semiconductor can be recrystallized.

***Response to Arguments***

12. Applicant's arguments have been considered but are moot in view of the new grounds of rejection.

***Conclusion***

No claims are allowable.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vanessa Velasquez whose telephone number is 571-270-3587. The examiner can normally be reached on Monday-Friday 9:00 AM-6:00 PM ET.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Roy King, can be reached at 571-272-1244. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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